



PRODUCT SPECIFICATION

Doc. Number:

- ☐ Tentative Specification
☐ Preliminary Specification
☒ Approval Specification

MODEL NO.: N156HRA
SUFFIX: GAA
DPN: YMHW H Rev.:C1

Customer: Dell**APPROVED BY****SIGNATURE****Name / Title**

Note

Please return 1 copy for your confirmation with your signature and comments.

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REVISION HISTORY

Version	Date	Page	Description
1.0	2019/12/23	ALL	Spec Ver. 1.0 was first issued.
2.0	2020/02/21	ALL	Spec Ver. 2.0 was first issued.
2.1	2020/03/26	33~36	revise EDID as new forma
2.2	2020/04/24	23	Change freesync operating range
3.0	2020/06/12	ALL	Spec Ver. 3.0 was first issued.
3.1	2021/09/16	33~36, 25~26	revise EDID as new forma & DP/N



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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N156HRA-GAA is a 15.6" (15.6" diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins eDP interface. This module supports 1920 x 1080 FHD mode and can display 16,777,216 colors.

1.2 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	15.6" diagonal	inch	-
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch	0.17925 (H) x 0.17925 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16,777,216	color	-
Interface	eDP 1.3	-	-
Transmissive Mode	Normally Black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	250	Cd/m2	-
Color Gamma	45%	NTSC	-
Power Consumption	Total 4.499W (Max.)@cell 1.419W (Max.), BL 3.08W (Max.)		(1)
Special Function	Freesync premium (support) PSR (PSR1 support)		-

Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 120 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 °C, whereas black pattern is displayed.

Note (2) Display port interface signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.3 (eDP1.3). There are many optional items described in eDP1.3. If some optional item is requested, please contact us.

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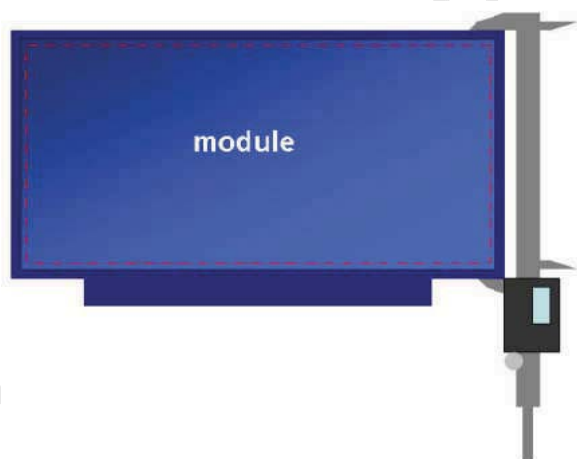
2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Glass	Thickness	-	0.4	-	mm	-
Polarizer	Thickness	-	0.135	-	mm	-
Module Size	Horizontal (H)	350.36	350.66	350.96	mm	(1) (2) (3)
	Vertical (V) w/o PCB and Hinge	204.94	205.24	205.54	mm	
	Vertical (V) with PCB w/o Hinge	215.75	216.25	216.75	mm	
	Thickness (T) w/o sponge	-	3.00	3.20	mm	
	Thickness (T) with sponge	-	-	-	mm	
Bezel Area	Horizontal	-	346.76	-	mm	-
	Vertical	-	196.59	-	mm	-
Active Area	Horizontal	344.06	344.16	344.26	mm	-
	Vertical	193.49	193.59	193.69	mm	-
Weight		-	350	365	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Dimensions are measured by caliper.

Note (3) Panel thickness is measured with calipers clamping mylar or tape tightly



2.1 CONNECTOR TYPE

Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12

User's connector Part No: IPEX-20453-040T-03



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3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

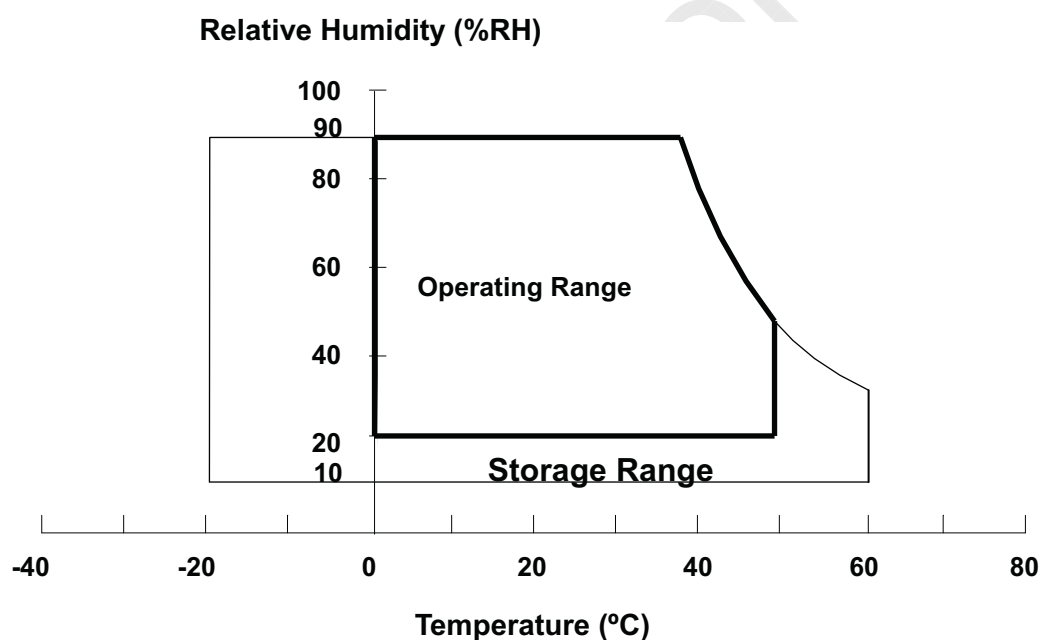
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)

Note (1) (a) 90 %RH Max. (Ta < 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta < 40 °C).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 °C min. and 60 °C max.



3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	26.0	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

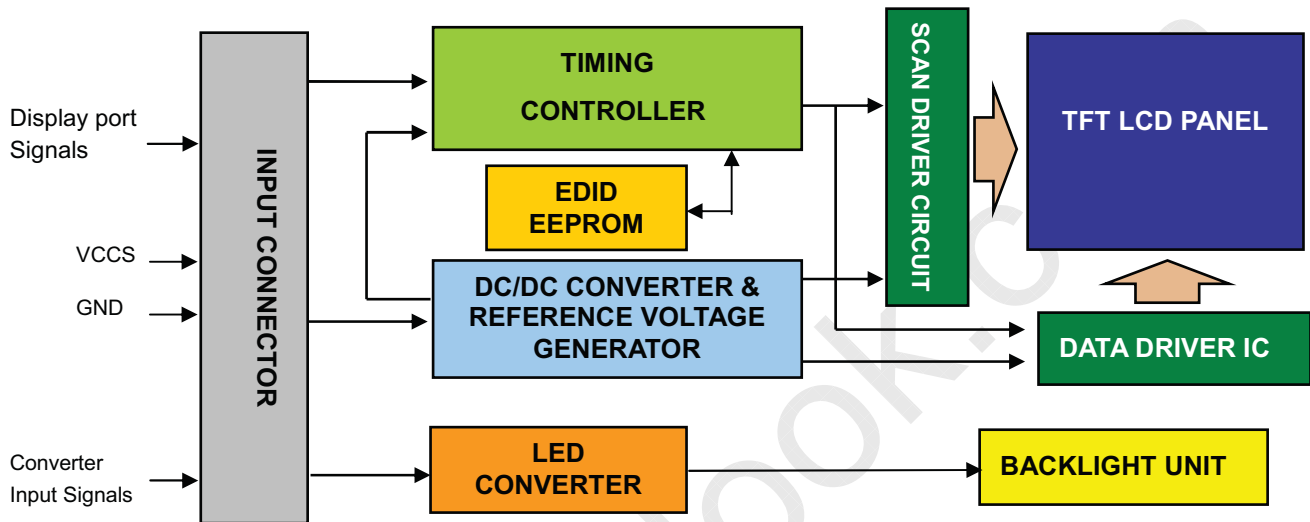
Note (1) Stresses beyond those listed in above "ELECTRICAL ABSOLUTE RATINGS" may cause

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permanent damage to the device. Normal operation should be restricted to the conditions described in "ELECTRICAL CHARACTERISTICS".

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2 INTERFACE CONNECTIONS

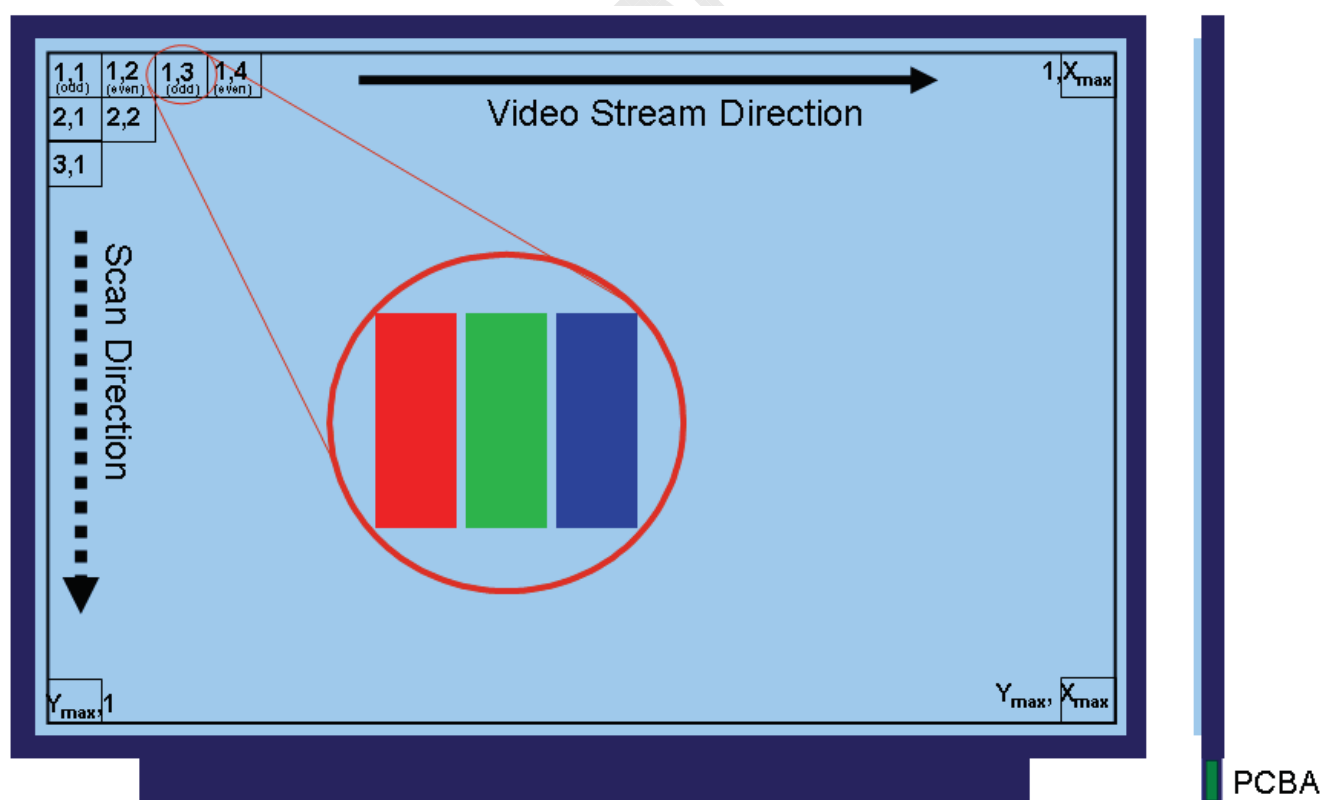
PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	Lane3_N	Complement Signal Link Lane 3	
4	Lane3_P	True Signal Link Lane 3	
5	H_GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane 2	
7	Lane2_P	True Signal Link Lane 2	
8	H_GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	H_GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	
13	Lane0_P	True Signal Link Lane 0	
14	H_GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	H_GND	High Speed Ground	
18	VCCS	LCD logic and driver power	
19	VCCS	LCD logic and driver power	
20	VCCS	LCD logic and driver power	

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21	VCCS	LCD logic and driver power	
22	BIST_EN	Panel Built In Self Test Enable	Note (2)
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	HPD	Hot Plug Detect	
28	BL_GND	Backlight ground	
29	BL_GND	Backlight ground	
30	BL_GND	Backlight ground	
31	BL_GND	Backlight ground	
32	LED_EN	BL_Enable Signal of LED Converter	
33	LED_PWM	PWM Dimming Control Signal of LED Converter	
34	NC	No Connection (Reserved for LCD test)	
35	NC	No Connection (Reserved for LCD test)	
36	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
37	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
38	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
39	LED_VCCS	Backlight power	(Support 5.0 ~ 21V)
40	NC	No Connection (Reserved for LCD test)	

Note (1) The first pixel is odd as shown in the following figure.



Note (2) The setting of CAB, BIST and Color engine function are as follows.

Pin	Enable	Disable
-----	--------	---------

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BIST_EN	Hi	Lo or Open
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Hi = High level, Lo = Low level.

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

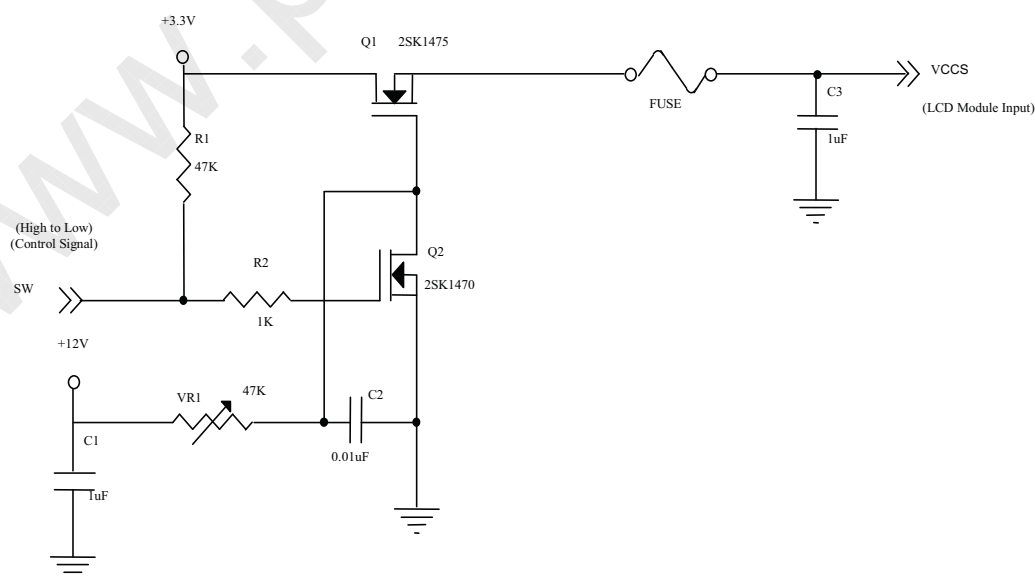
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)(7)
HPD	High Level	-	2.25	-	2.75	V	(6)
	Low Level	-	0	-	0.4	V	(6)
HPD Impedance		R _{HPD}	30K	-	-	ohm	(5)
Ripple Voltage		V _{RP}	-	-	100	mV	(1)
Inrush Current		I _{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Black	I _{CC}	-	390	430	mA	(3)
	Mosaic		-	405	445	mA	(3)
	Solid Pattern		-	590.8	649.9	mA	(3)
	Mosaic @PSR		-	405	445	mA	(3)a
	Solid Pattern @ PSR		-	590.8	649.9	mA	(3)a
Power per EBL WG		P _{EBL}	-	2.09	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

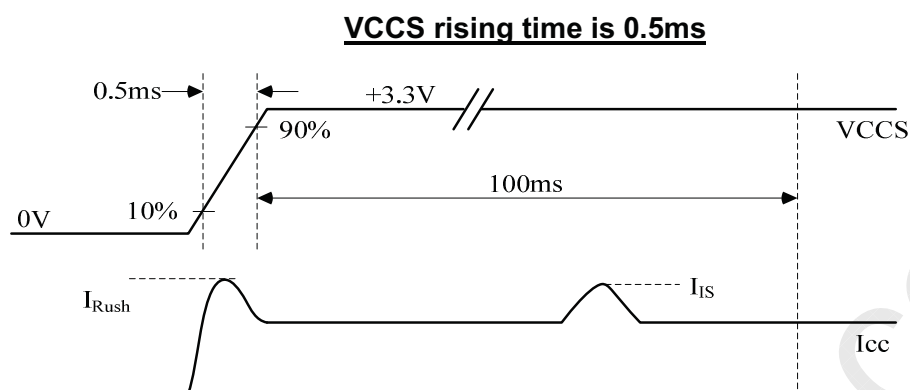
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.

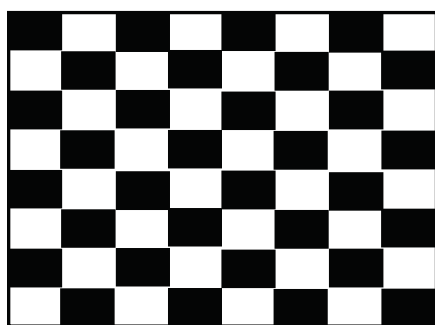


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Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and $f_v = 120\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

1. Mosaic Pattern



Active Area

2. The solid pattern is the largest one of R/G/B pattern..

Note(3)a The specified power supply current is under the conditions at VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, DC Current and PSR mode enable, whereas a power dissipation check pattern is displayed.

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

(a) VCCS = 3.3 V, $T_a = 25 \pm 2^\circ\text{C}$, $f_v = 120\text{ Hz}$,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits

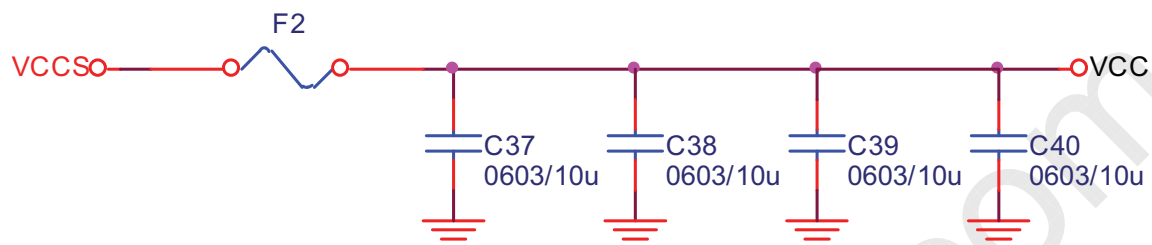
Note (5) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. Please refer to Note (4) of 4.3.2 LED CONVERTER SPECIFICATION to obtain more

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information.

Note (6) When a source detects a low-going HPD pulse, it must be regarded as a HPD event. Thus, the source must read the link / sink status field or receiver capability field of the DPCD and take corrective action

Note (7) Input VCC Circuit is as below



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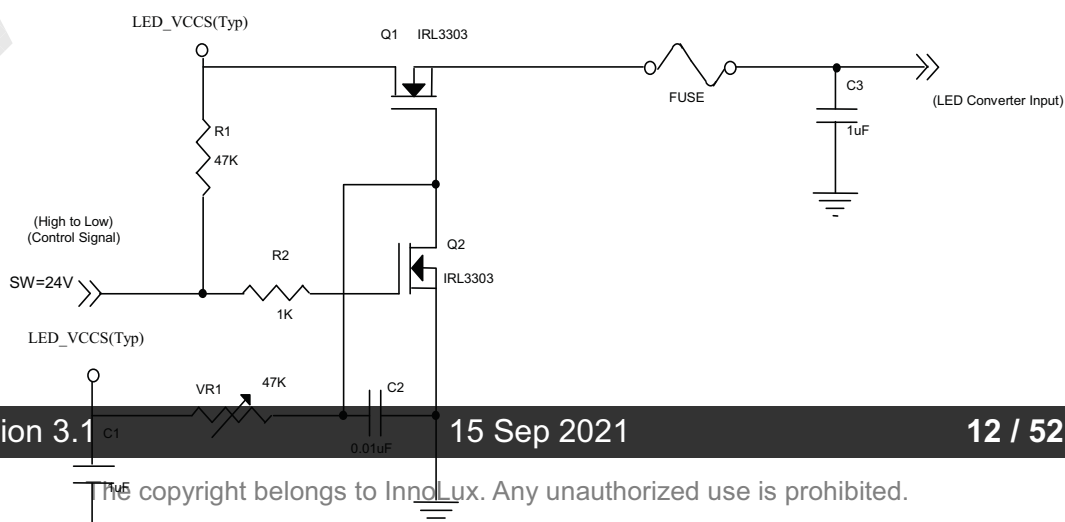
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input Power Supply Voltage		LED_Vccs	5.0	12.0	21.0	V	-
Converter Inrush Current		I _{LED_RUSH}	-	-	1.5	A	(1)
LED_EN Control Level	Backlight On	-	2.2	-	5.0	V	(4)
	Backlight Off		0	-	0.6	V	(4)
LED_EN Impedance		R _{LED_EN}	30K	-	-	ohm	(4)
PWM Control Level	PWM High Level	-	2.2	-	5	V	(4)
	PWM Low Level		0	-	0.6	V	(4)
PWM Impedance		R _{PWM}	30K	-	-	ohm	(4)
PWM Control Duty Ratio		-	5	-	100	%	(5)
PWM Control Permissive Ripple Voltage		V _{PWM_pp}	-	-	100	mV	-
PWM Control Frequency		f _{PWM}	190	-	2K	Hz	(2)
LED Power Current	LED_VCCS =Typ.	I _{LED}		246.33	256.66	mA	(3)

Note (1) I_{LED_RUSH}: the maximum current when LED_VCCS is rising,

I_{LED_IS}: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 °C, f_{PWM} = 200 Hz, Duty=100%.



Version 3.1

15 Sep 2021

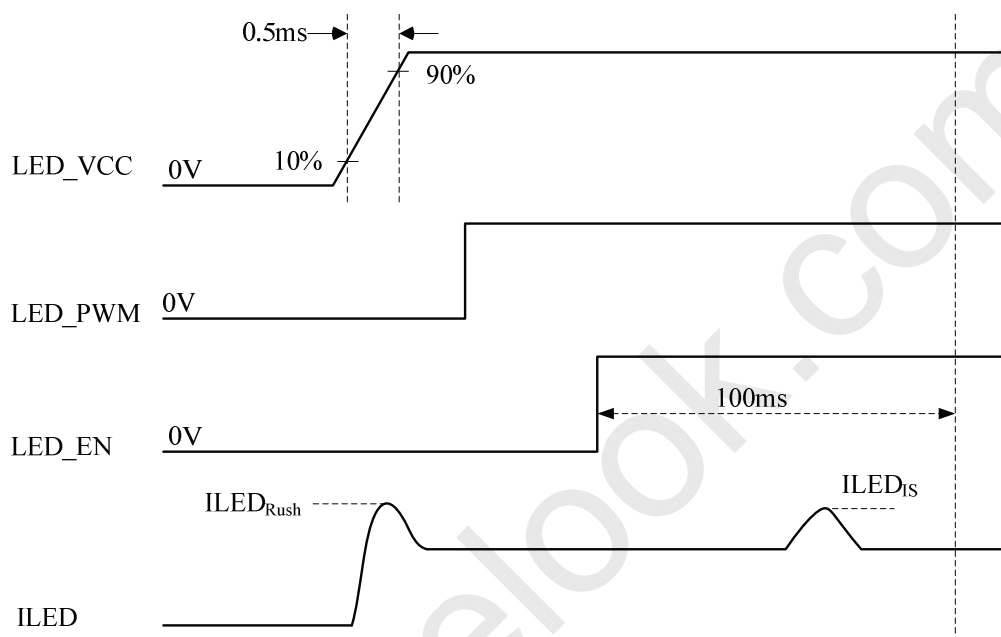
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VLED rising time is 0.5ms



Note (2) If PWM control frequency is applied in the range less than 1KHz, the “waterfall” phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N + 0.33) * f \leq f_{PWM} \leq (N + 0.66) * f$$

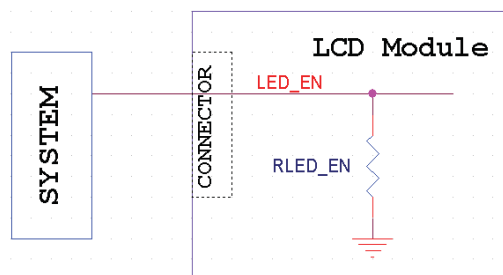
N : Integer ($N \geq 3$)

f : Frame rate

Note (3) The specified LED power supply current is under the conditions at “LED_VCCS = Typ.”, $T_a = 25 \pm 2^\circ\text{C}$, $f_{PWM} = 200\text{ Hz}$, Duty=100%.

Note (4) The specified signals have equivalent impedances pull down to ground in the LCD module respectively. Customers should keep the input signal level requirement with the load of LCD module. For example, the figure below describes the equivalent pull down impedance of LED_EN (If it exists). The rest pull down impedances of other signals (eg. HPD, PWM ...) are in the same concept.

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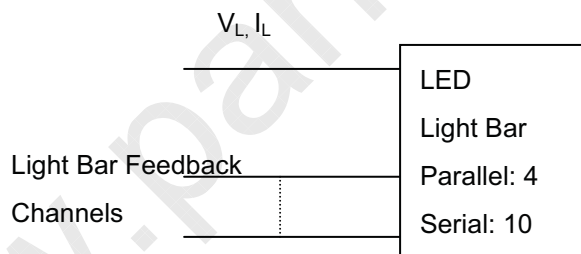
Note (5) If the cycle-to-cycle difference of PWM duty exceeds 0.1%, especially when the PWM duty is low, slight brightness change might be observed.

4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V _L	27	29	30	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I _L	--	88	--	mA	(3)
Power Consumption	P _L	--	2.552	2.64	W	
LED Life Time	L _{BL}	15000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and I_L = 22 mA(Per EA) until the brightness becomes ≤ 50% of its original value.

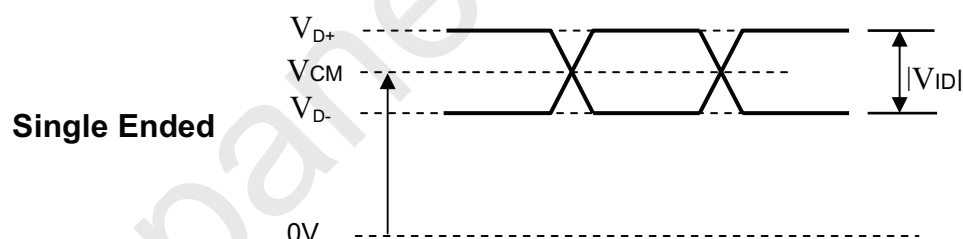
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4.4 DISPLAY PORT SIGNAL TIMING SPECIFICATION

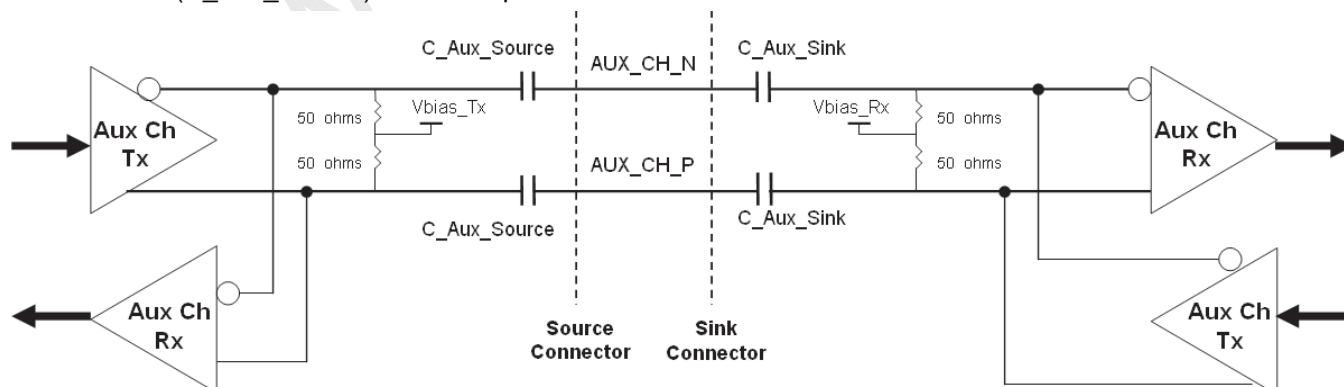
4.4.1 ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0	-	2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75	-	200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75	-	200	nF	(3)

Note (1)Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.

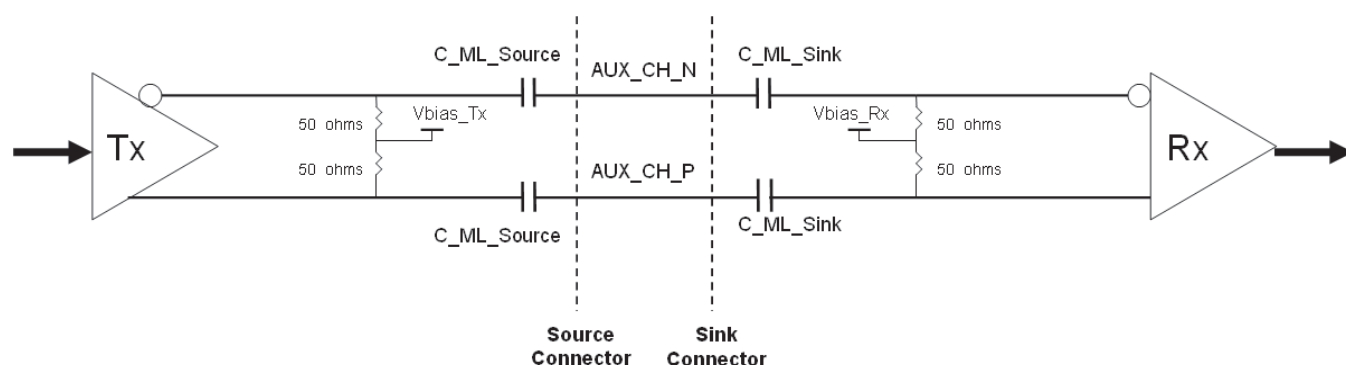


(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.

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(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Refresh Rate 120Hz

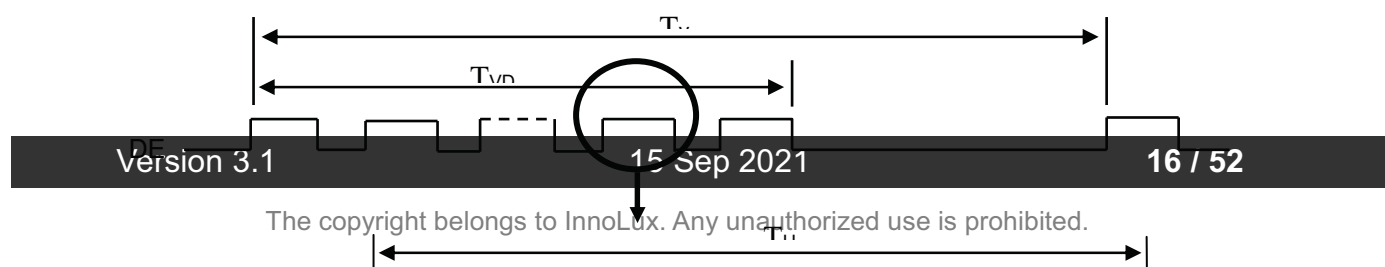
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	281.31	285.04	288.79	MHz	-
DE	Vertical Total Time	TV	1138	1142	1146	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	62	TV-TVD	TH	-
	Horizontal Total Time	TH	2060	2080	2100	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Refresh rate 60Hz (Power Saving Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	281.8	285.04	288.29	MHz	(1)
DE	Vertical Total Time	TV	2280	2284	2288	TH	(1)
	Vertical Active Display Period	TVD	1080	1080	1080	TH	(1)
	Vertical Active Blanking Period	TVB	TV-TVD	1204	TV-TVD	TH	(1)
	Horizontal Total Time	TH	2060	2080	2100	Tc	(1)
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	(1)
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	(1)

Note (1) The panel can operate at 120Hz normal mode and power saving mode, respectively. All reliability tests are based on specific timing of 120Hz refresh rate. We can only assure the panel's electrical function at power saving mode.

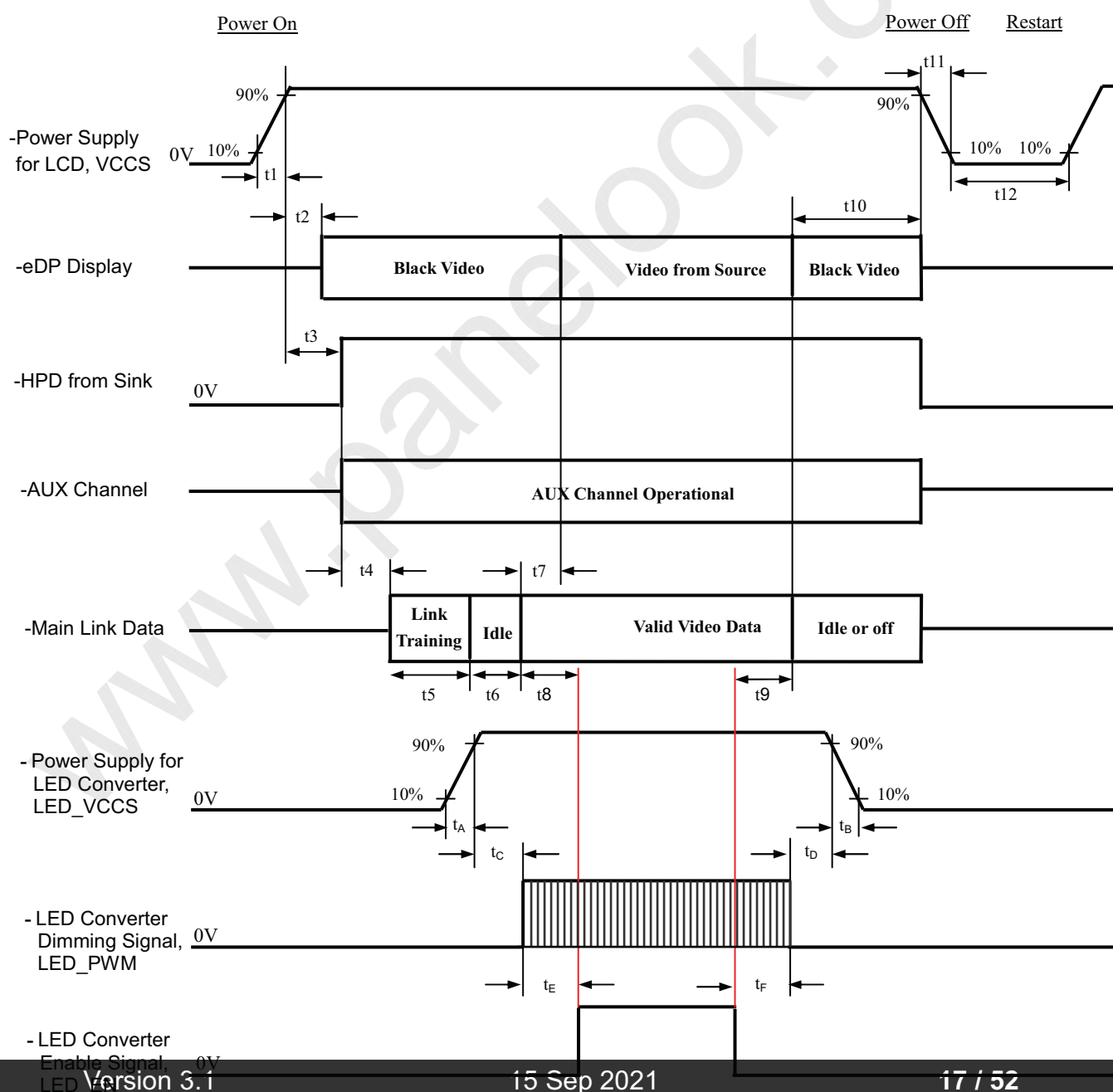
INPUT SIGNAL TIMING DIAGRAM



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4.6 POWER ON/OFF SEQUENCE





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Timing Specifications

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	0	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	0	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	0	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	80	-	ms	Source must assure display video is stable *: Recommended by INX. To avoid garbage image.
t9	Delay from backlight off to end of valid video data	Source	50	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below) *: Recommended by INX. To avoid garbage image.
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-

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t ₁₂	VCCS Power off time	Source	500	-	ms	-
t _A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t _B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-
t _C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t _D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t _E	Delay from LED dimming signal to LED enable signal	Source	(0)	-	ms	-
t _F	Delay from LED enable signal to LED dimming signal	Source	(0)	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on. Before LCD_VCCS and LED_VCCS are ready, it is recommended to pull down the backlight control signals.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.



PRODUCT SPECIFICATION

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	88	mA

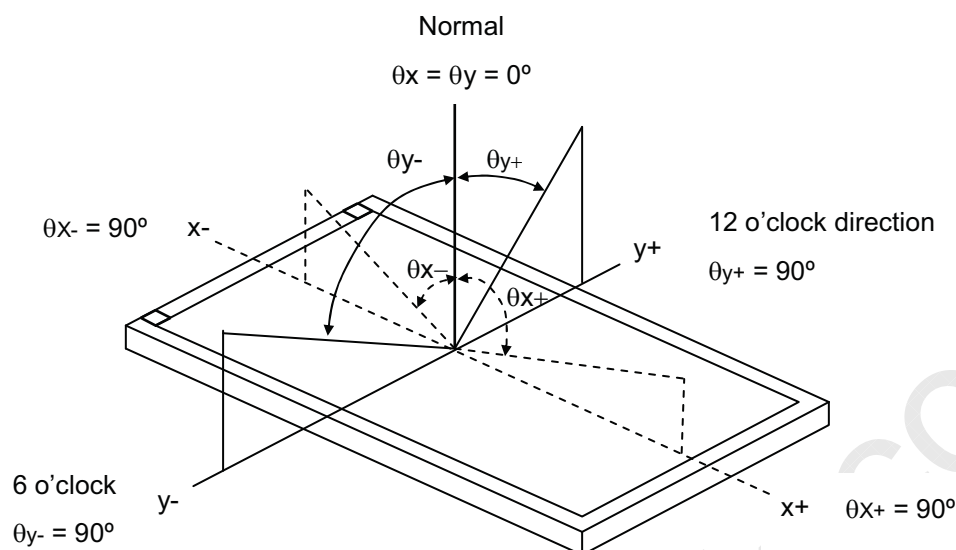
The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_Y=0^\circ$ Viewing Normal Angle	800	1000	-	-	(2), (5),(7)
Response Time		T _R		-	11	14	ms	(3),(7)
		T _F		-	9	11	ms	
Average Luminance of White		L _{Ave}		212	250	-	cd/m ²	(4), (6),(7)
Color Chromaticity	Red	R _x		Typ – 0.03	Typ + 0.03	-	(1),(7)	
		R _y				-		
	Green	G _x				-		
		G _y				-		
	Blue	B _x				-		
		B _y				-		
	White	W _x				-		
		W _y				-		
	Color Gamut	C.G.		42	45	-	-	(8)
Viewing Angle	Horizontal	θ_x+	CR≥10	80	89	-	Deg.	(1),(5), (7)
		θ_x-		80	89	-		
	Vertical	θ_Y+		80	89	-		
		θ_Y-		80	89	-		
White Variation of 5 and 13 Points		δW_{5p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	80	90	-	%	(5),(6)
		δW_{13p}	$\theta_x=0^\circ, \theta_Y=0^\circ$	65	75	-	%	(7)

PRODUCT SPECIFICATION

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

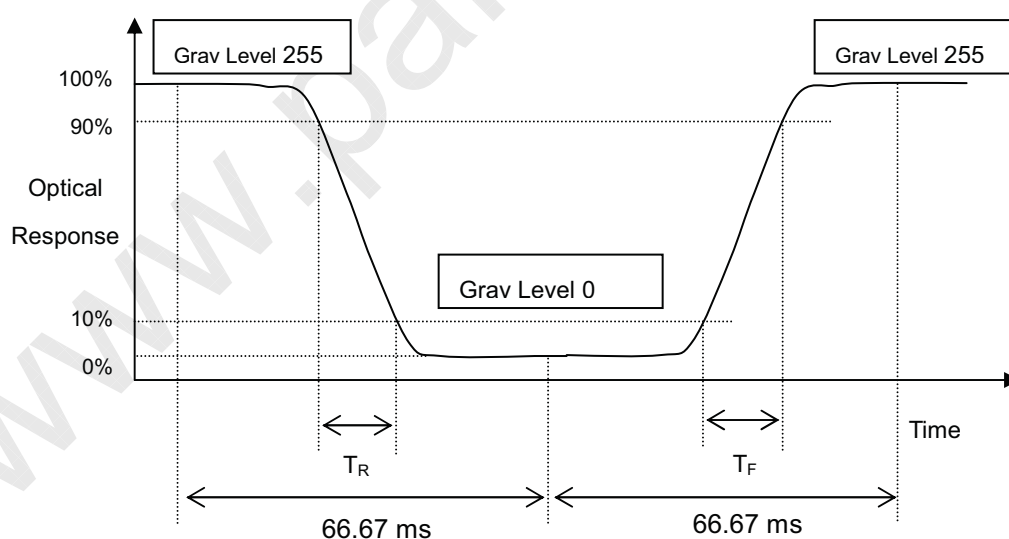
L_{255} : Luminance of gray level 255

L_0 : Luminance of gray level 0

$$CR = CR(1)$$

$CR(X)$ is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of White at 5 points

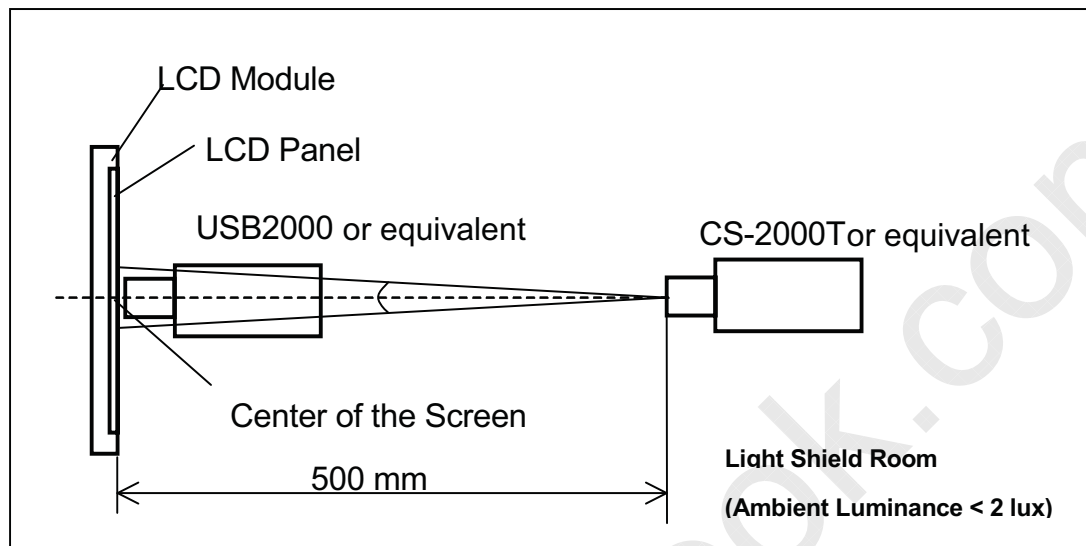
$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (6)

PRODUCT SPECIFICATION

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

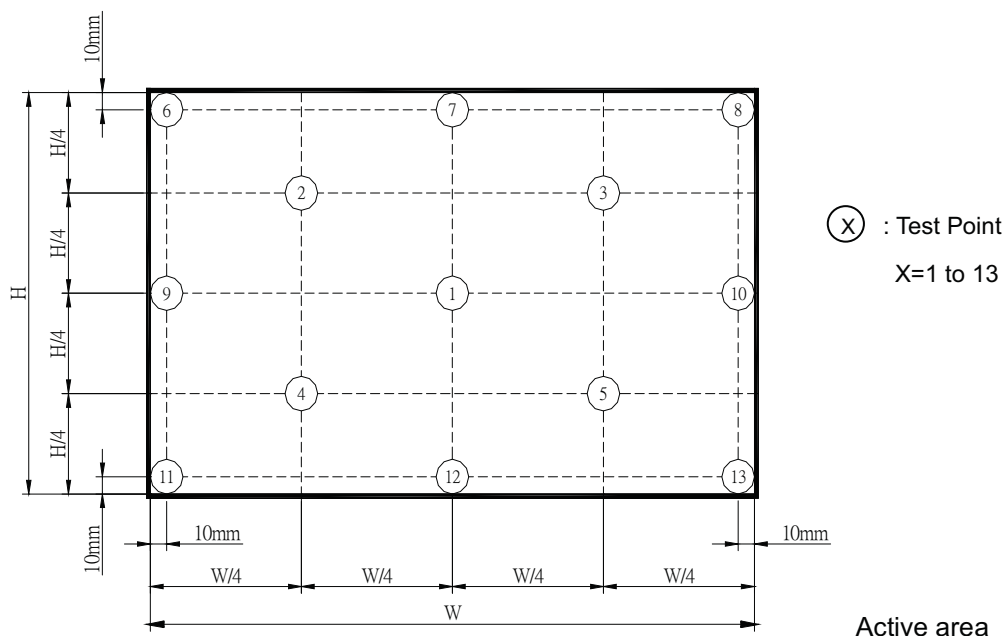


Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points / 13 points

$$\delta W_{5p} = \{ \text{Minimum } [L(1) \sim L(5)] / \text{Maximum } [L(1) \sim L(5)] \} * 100\%$$

$$\delta W_{13p} = \{ \text{Minimum } [L(1) \sim L(13)] / \text{Maximum } [L(1) \sim L(13)] \} * 100\%$$



Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

PRODUCT SPECIFICATION

Note (8) Definition of color gamut (C.G%):

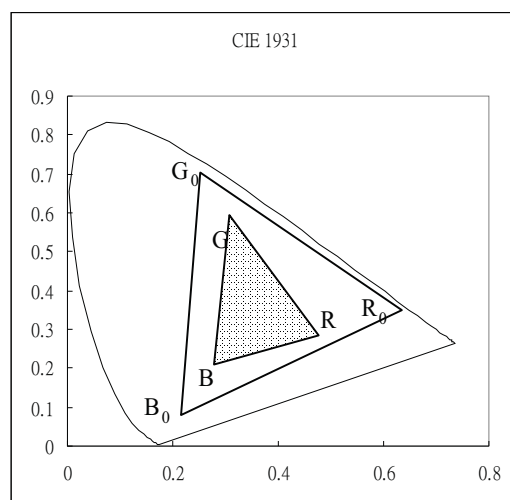
$$C.G\% = \frac{R G B}{R_0 G_0 B_0} \times 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 255 gray levels of red, green, and blue, respectively.

$R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$R G B$: area of triangle defined by R, G, B



PRODUCT SPECIFICATION

6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	60°C, 240 hours	(1) (2)
Low Temperature Storage Test	-20°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5hour $\longleftrightarrow$ 60°C, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	50°C, 240 hours	
Low Temperature Operation Test	0°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, 80% RH, 240 hours	(1)
ESD Test (Operation)	150pF, 330 Ω , 1sec/cycle Condition 1 : Contact Discharge, ± 8 KV Condition 2 : Air Discharge, ± 15 KV	
Shock (Non-Operating)	220G, 2ms, half sine wave, 1 time for each direction of $\pm X, \pm Y, \pm Z$	
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

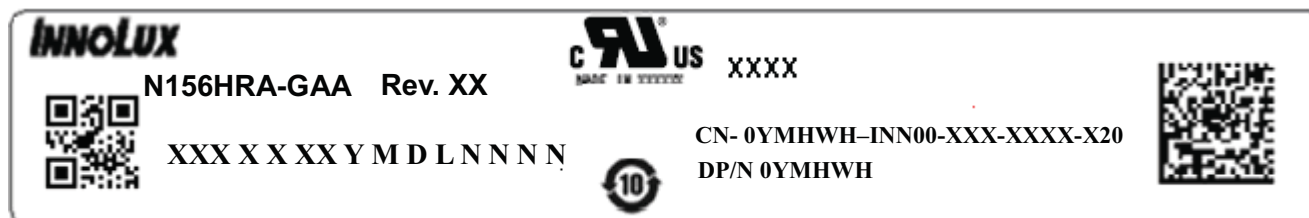
Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

PRODUCT SPECIFICATION

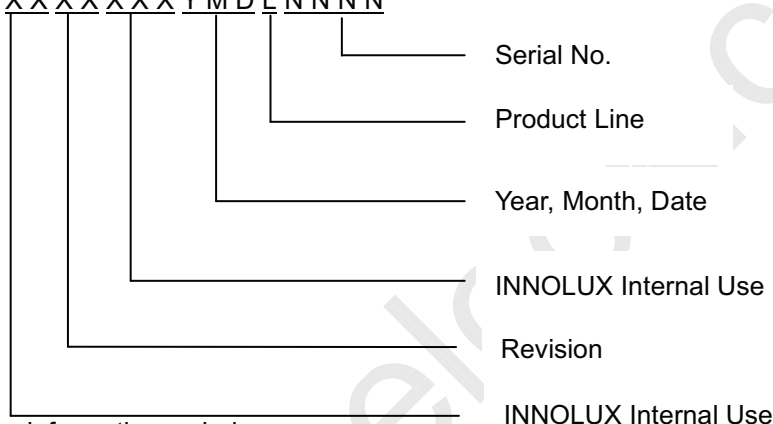
7. PACKING

7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



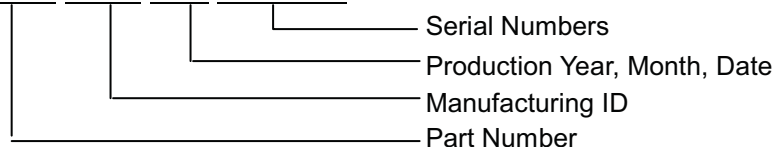
- (a) Model Name: N156HRA-GAA
- (b) Revision: Rev. XX, for example: C1, C2 ...etc.
- (c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 0~9, for 2010~2019
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product
- (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.
- (e) UL Logo : XXXX is UL factory ID.
- (f) Dell 2D label contains information as below:

(f-1) Serial ID: CN-0SSSSS-INN00-YMD-XXXX-ZZZ



(f-1-1) Corresponding LCM Fab code XXXXX is as below

-INN00 : Ningbo F2

(f-2) Production location: Made in XXXX.

(f-3) ZZZ:Revision code: X00, X10, X20, A00..etc.

PRODUCT SPECIFICATION

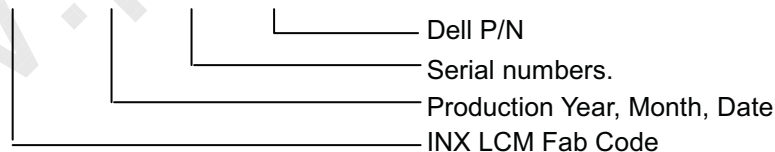
BUILD PHASE	REVISION
SST (WS)	X00, X01, X02, ... X09
PT (ES)	X10, X11, X12, ... X19
ST (CS)	X20, X21, X23, ... X29
XB (MP)	A00, A01, A02, ... A99

7.2 DELL Carton Label

Dell carton label contains information as below:



(a) PKG ID: 04688-XXXXX-YMD-XXXXXX-0SSSSS-ZZ



(b) Production location: Made in XXXX.

(c) Revision code: X00, X10, X20, A00..etc.

(d) BOX Quantity: ZZ

(e) DILoc ID&Mfg ID XXXXX INX LCM Fab Code

(e-1) Corresponding LCM Fab code XXXXX is as below

- INT00: J001&J003 Tainan
- IN200: Ningbo, No.16, YangZi River North Rd., Ningbo Export Processing Zone
- INN00: Ningbo F2 ,No.6, YangZiJiang South Road, Ningbo Export Processing Zone
- INZ00: Ningbo F3&F4, No.9, YangZiJiang North Road, Ningbo Bonded Zone

PRODUCT SPECIFICATION

7.3 CARTON

- (1) Box Dimensions : 500(L)*370(W)*270(H)
 (2) 20 modules/Carton

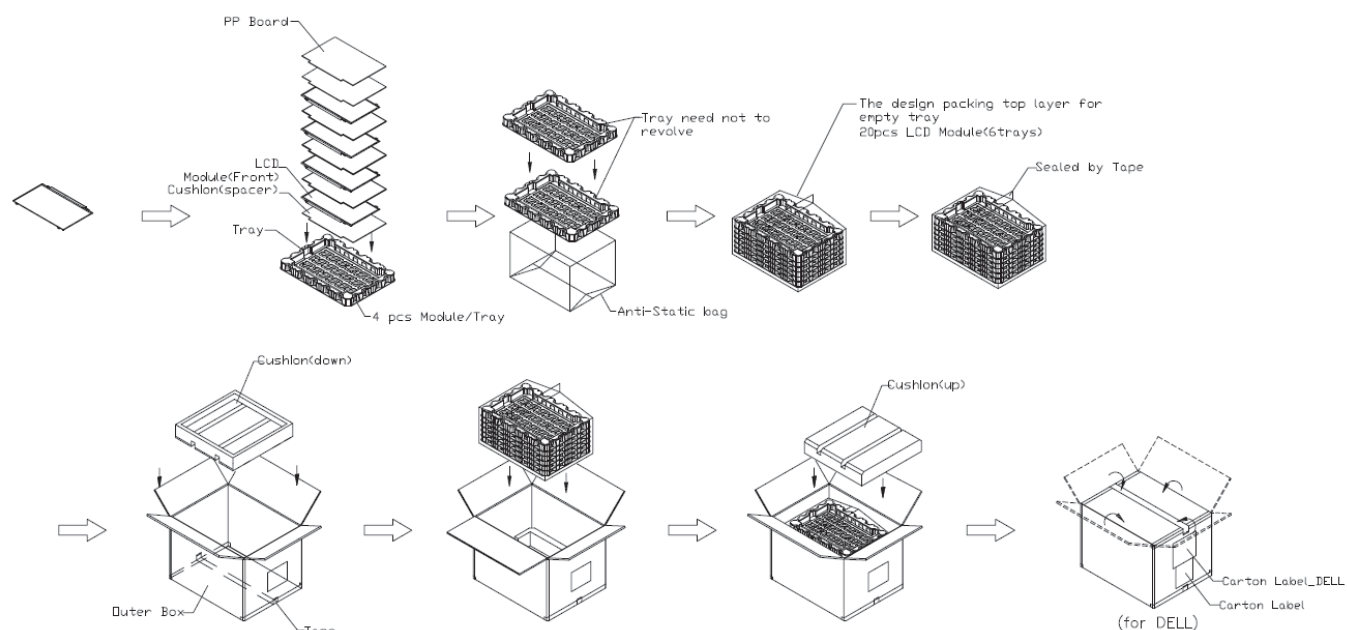
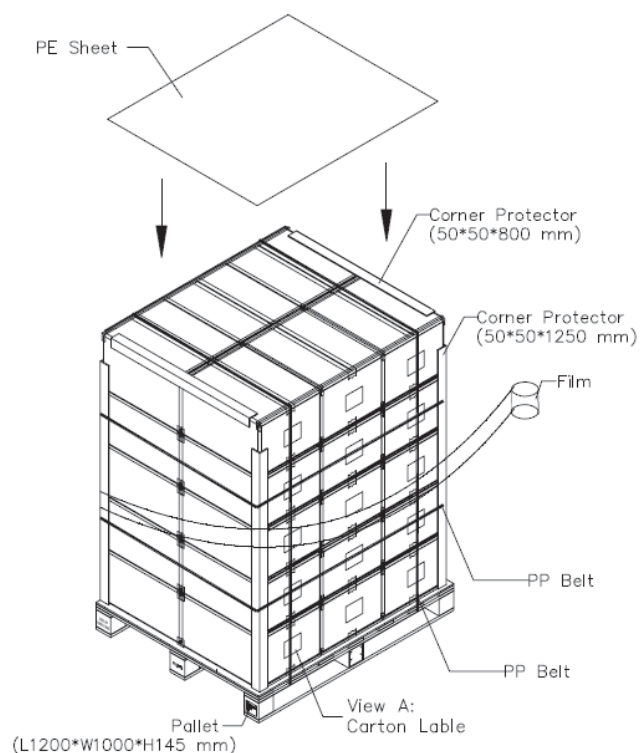


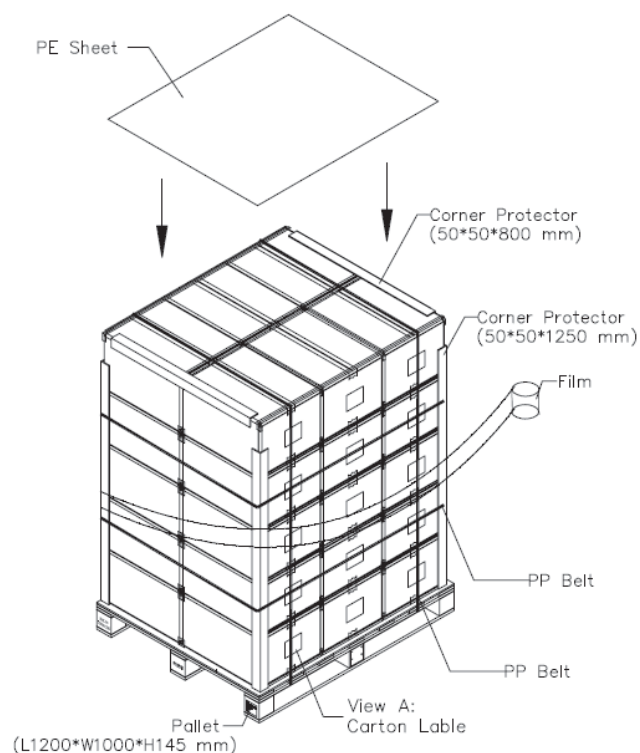
Figure. 7-1 Packing method

PRODUCT SPECIFICATION

7.4 PALLET



Sea & Land Transportation



Air Transportation

Figure. 7-2 Packing method

PRODUCT SPECIFICATION

7.5 UN-PACKAGING METHOD

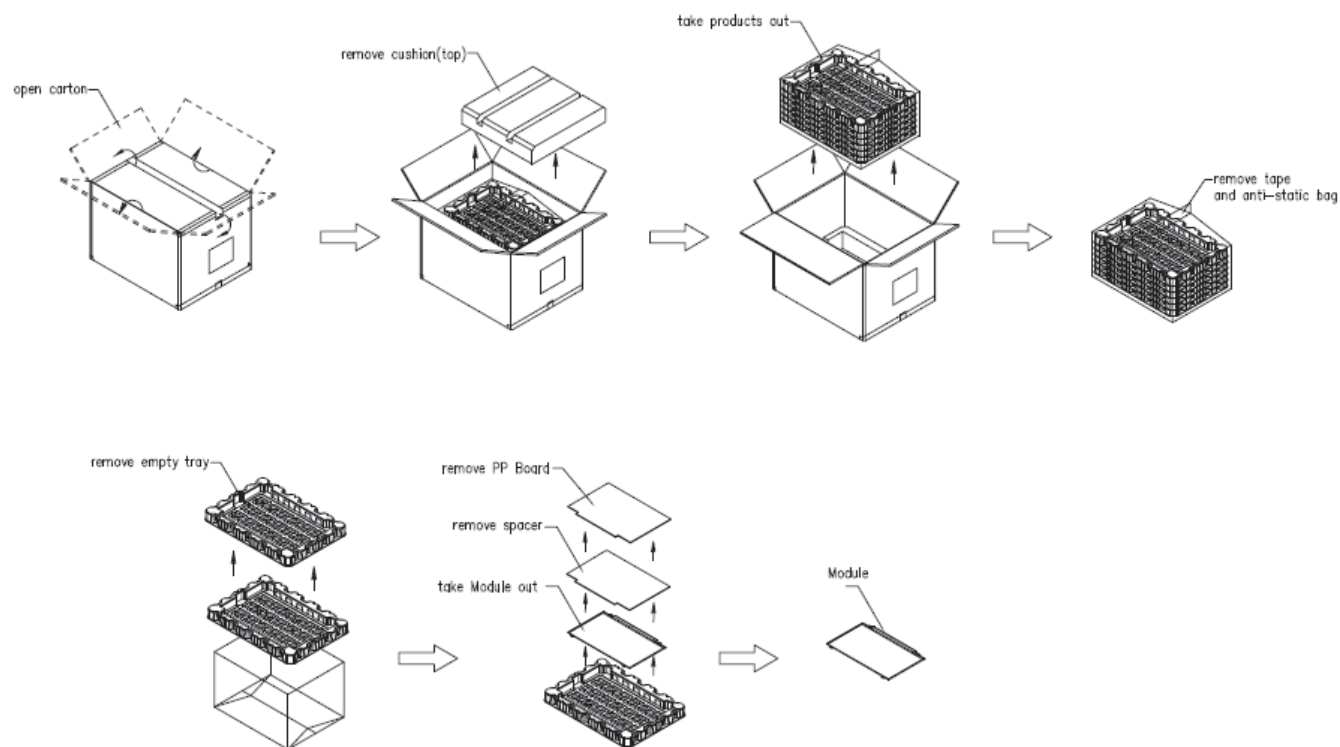


Figure. 7-3 Un-packing method



PRODUCT SPECIFICATION

8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the LED wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.



PRODUCT SPECIFICATION

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	ID system manufacturer name ("CMN")	0D	00001101
9	9	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	22	00100010
11	0B	ID system Product Code (MSB)	15	00010101
12	0C	ID S/N (fixed "00")	00	00000000
13	0D	ID S/N (fixed "00")	00	00000000
14	0E	ID S/N (fixed "00")	00	00000000
15	0F	ID S/N (fixed "00")	00	00000000
16	10	Week of manufacture (fixed week code)	16	00010110
17	11	Year of manufacture (fixed year code)	1E	00011110
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	A5	10100101
21	15	Active area horizontal ("34.416cm")	22	00100010
22	16	Active area vertical ("19.359cm")	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	03	00000011
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	28	00101000
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	65	01100101
27	1B	Rx=0.59	97	10010111
28	1C	Ry=0.35	59	01011001
29	1D	Gx=0.33	54	01010100
30	1E	Gy=0.555	8E	10001110
31	1F	Bx=0.153	27	00100111
32	20	By=0.119	1E	00011110
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001



PRODUCT SPECIFICATION

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("285.08MHz")	5C	01011100
55	37	# 1 Pixel clock (hex LSB first)	6F	01101111
56	38	# 1 H active ("1920")	80	10000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank	70	01110000
59	3B	# 1 V active ("1080")	38	00111000
60	3C	# 1 V blank ("62")	3E	00111110
61	3D	# 1 V active : V blank	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("10 :5")	A5	10100101
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size ("344 mm")	58	01011000
67	43	# 1 V image size ("193 mm")	C1	11000001
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 Data Type Tag	FD	11111101
76	4C	# 2 FreeSync Setting - Display Range Limits Offset V : H ("0 : 0")	00	00000000
77	4D	# 2 FreeSync Setting - Minimum Vertical Rate ("48Hz")	30	00110000
78	4E	# 2 FreeSync Setting - Maximum Vertical Rate ("120Hz")	78	01111000
79	4F	# 2 FreeSync Setting - Minimum Horizontal Rate ("137kHz")	89	10001001
80	50	# 2 FreeSync Setting - Maximum Horizontal Rate ("137kHz")	89	10001001
81	51	# 2 FreeSync Setting - Maximum Pixel Clocks ("285MHz")	1D	00011101
82	52	# 2 FreeSync Setting - Video Timing Support Flag ("Range Limit Only")	01	00000001
83	53	# 2 FreeSync Setting ("Line Feed")	0A	00001010
84	54	# 2 Padding with "Blank" character	20	00100000
85	55	# 2 Padding with "Blank" character	20	00100000
86	56	# 2 Padding with "Blank" character	20	00100000
87	57	# 2 Padding with "Blank" character	20	00100000



PRODUCT SPECIFICATION

88	58	# 2 Padding with "Blank" character	20	00100000
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
94	5E	Flag	00	00000000
95	5F	Dell P/N 1st Character "Y"	59	00110111
96	60	Dell P/N 2nd Character "M"	4D	01011000
97	61	Dell P/N 3rd Character "H"	48	01000111
98	62	Dell P/N 4th Character "W"	57	01001110
99	63	Dell P/N 5th Character "H"	48	01001010
100	64	EDID Revision	80	10000000
101	65	Manufacturer P/N "1"	31	00110001
102	66	Manufacturer P/N "5"	35	00110101
103	67	Manufacturer P/N "6"	36	00110110
104	68	Manufacturer P/N "H"	48	01001000
105	69	Manufacturer P/N "R"	52	01010010
106	6A	Manufacturer P/N "A"	41	01000001
107	6B	New line character indicates end of ASCII string	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
112	70	Flag	00	00000000
113	71	Color Management	01	00000001
114	72	Panel Type and Revision	41	01000001
115	73	Frame Rate	0F	00001111
116	74	Light Controller Interface and Maximum Luminance	99	10011001
117	75	Front Surface / Polarizer and Pixel Structure	00	00000000
118	76	Multi-Media Features	10	00010000
119	77	Multi-Media Features	00	00000000
120	78	Special Features	00	00000000
121	79	Special Features	0B	00001011
122	7A	Special Features	01	00000001
123	7B	New line character indicates end of ASCII string	0A	00001010
124	7C	Padding with "Blank" character	20	00100000
125	7D	Padding with "Blank" character	20	00100000
126	7E	No extension	01	00000001
127	7F	Checksum	88	10001000
128	80	DisplayID EDID extension block tag	70	01110000
129	81	DisplayID version revision	13	00010011
130	82	section size	79	01111001
131	83	product type identifier	00	00000000
132	84	extension count	00	00000000
133	85	data block tag = type 1 timing detailed	03	00000011
134	86	block revision = 01	01	00000001



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135	87	Number of payload bytes in block = (N x 20), 1<=N<=12	14	00010100
136	88	Pixel Clk/10,000 [low bit]	5C	01011100
137	89	Pixel Clk/10,000 [middle bit]	6F	01101111
138	8A	Pixel Clk/10,000 [high bit]	00	00000000
139	8B	timing option [prefered "detaild" timing, No streeo, 16:9']	04	00000100
140	8C	Horizontal Active [low bit]	7F	01111111
141	8D	Horizontal Active [high bit]	07	00000111
142	8E	Horizontal blank [low bit]	9F	10011111
143	8F	Horizontal blank [high bit]	00	00000000
144	90	Horizontal offset (front porch) [low bit]	2F	00101111
145	91	Horizontal offset (front porch) [high bit] / Horizontal sync polarity = Positive	00	00000000
146	92	Horizontal Sync width [low bit]	1F	00011111
147	93	Horizontal Sync width [high bit]	00	00000000
148	94	Vertical Active [low bit]	37	00110111
149	95	Vertical Active [high bit]	04	00000100
150	96	Vertical blank [low bit]	B4	10110100
151	97	Vertical blank [high bit]	04	00000100
152	98	Vertical offset (front porch) [low bit]	09	00001001
153	99	Vertical offset (front porch) [high bit] / Vertical sync polarity = Negative	00	00000000
154	9A	Vertical Sync width [low bit]	04	00000100
155	9B	Vertical Sync width [high bit]	00	00000000
156	9C	Reserved	00	00000000
157	9D	Reserved	00	00000000
158	9E	Reserved	00	00000000
159	9F	Reserved	00	00000000
160	A0	Reserved	00	00000000
161	A1	Reserved	00	00000000
162	A2	Reserved	00	00000000
163	A3	Reserved	00	00000000
164	A4	Reserved	00	00000000
165	A5	Reserved	00	00000000
166	A6	Reserved	00	00000000
167	A7	Reserved	00	00000000
168	A8	Reserved	00	00000000
169	A9	Reserved	00	00000000
170	AA	Reserved	00	00000000
171	AB	Reserved	00	00000000
172	AC	Reserved	00	00000000
173	AD	Reserved	00	00000000
174	AE	Reserved	00	00000000
175	AF	Reserved	00	00000000
176	B0	Reserved	00	00000000
177	B1	Reserved	00	00000000
178	B2	Reserved	00	00000000
179	B3	Reserved	00	00000000
180	B4	Reserved	00	00000000
181	B5	Reserved	00	00000000



PRODUCT SPECIFICATION

182	B6	Reserved	00	00000000
183	B7	Reserved	00	00000000
184	B8	Reserved	00	00000000
185	B9	Reserved	00	00000000
186	BA	Reserved	00	00000000
187	BB	Reserved	00	00000000
188	BC	Reserved	00	00000000
189	BD	Reserved	00	00000000
190	BE	Reserved	00	00000000
191	BF	Reserved	00	00000000
192	C0	Reserved	00	00000000
193	C1	Reserved	00	00000000
194	C2	Reserved	00	00000000
195	C3	Reserved	00	00000000
196	C4	Reserved	00	00000000
197	C5	Reserved	00	00000000
198	C6	Reserved	00	00000000
199	C7	Reserved	00	00000000
200	C8	Reserved	00	00000000
201	C9	Reserved	00	00000000
202	CA	Reserved	00	00000000
203	CB	Reserved	00	00000000
204	CC	Reserved	00	00000000
205	CD	Reserved	00	00000000
206	CE	Reserved	00	00000000
207	CF	Reserved	00	00000000
208	D0	Reserved	00	00000000
209	D1	Reserved	00	00000000
210	D2	Reserved	00	00000000
211	D3	Reserved	00	00000000
212	D4	Reserved	00	00000000
213	D5	Reserved	00	00000000
214	D6	Reserved	00	00000000
215	D7	Reserved	00	00000000
216	D8	Reserved	00	00000000
217	D9	Reserved	00	00000000
218	DA	Reserved	00	00000000
219	DB	Reserved	00	00000000
220	DC	Reserved	00	00000000
221	DD	Reserved	00	00000000
222	DE	Reserved	00	00000000
223	DF	Reserved	00	00000000
224	E0	Reserved	00	00000000
225	E1	Reserved	00	00000000
226	E2	Reserved	00	00000000
227	E3	Reserved	00	00000000
228	E4	Reserved	00	00000000



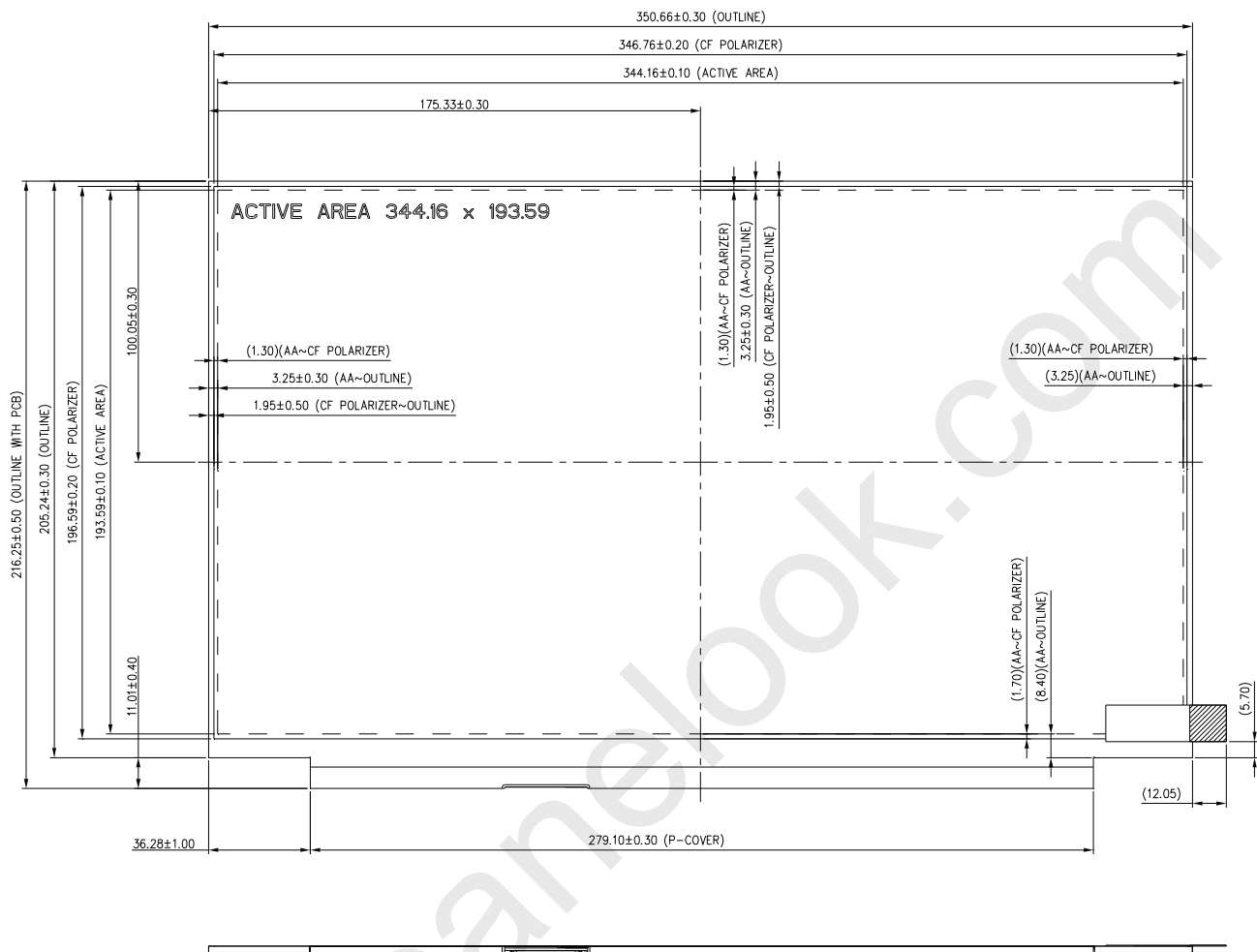
PRODUCT SPECIFICATION

224	E0	Reserved	00	00000000
225	E1	Reserved	00	00000000
226	E2	Reserved	00	00000000
227	E3	Reserved	00	00000000
228	E4	Reserved	00	00000000
224	E0	Reserved	00	00000000
225	E1	Reserved	00	00000000
226	E2	Reserved	00	00000000
227	E3	Reserved	00	00000000
228	E4	Reserved	00	00000000
224	E0	Reserved	00	00000000
240	F0	Reserved	00	00000000
241	F1	Reserved	00	00000000
242	F2	Reserved	00	00000000
243	F3	Reserved	00	00000000
244	F4	Reserved	00	00000000
245	F5	Reserved	00	00000000
246	F6	Reserved	00	00000000
247	F7	Reserved	00	00000000
248	F8	Reserved	00	00000000
249	F9	Reserved	00	00000000
250	FA	Reserved	00	00000000
251	FB	Reserved	00	00000000
252	FC	Reserved	00	00000000
253	FD	Reserved	00	00000000
254	FE	DID Section Checksum	1A	00011010
255	FF	EDID Extension Block Checksum	90	10010000

Note1: The data at E0h~EFh are used for INX to record the serial number of the product.

PRODUCT SPECIFICATION

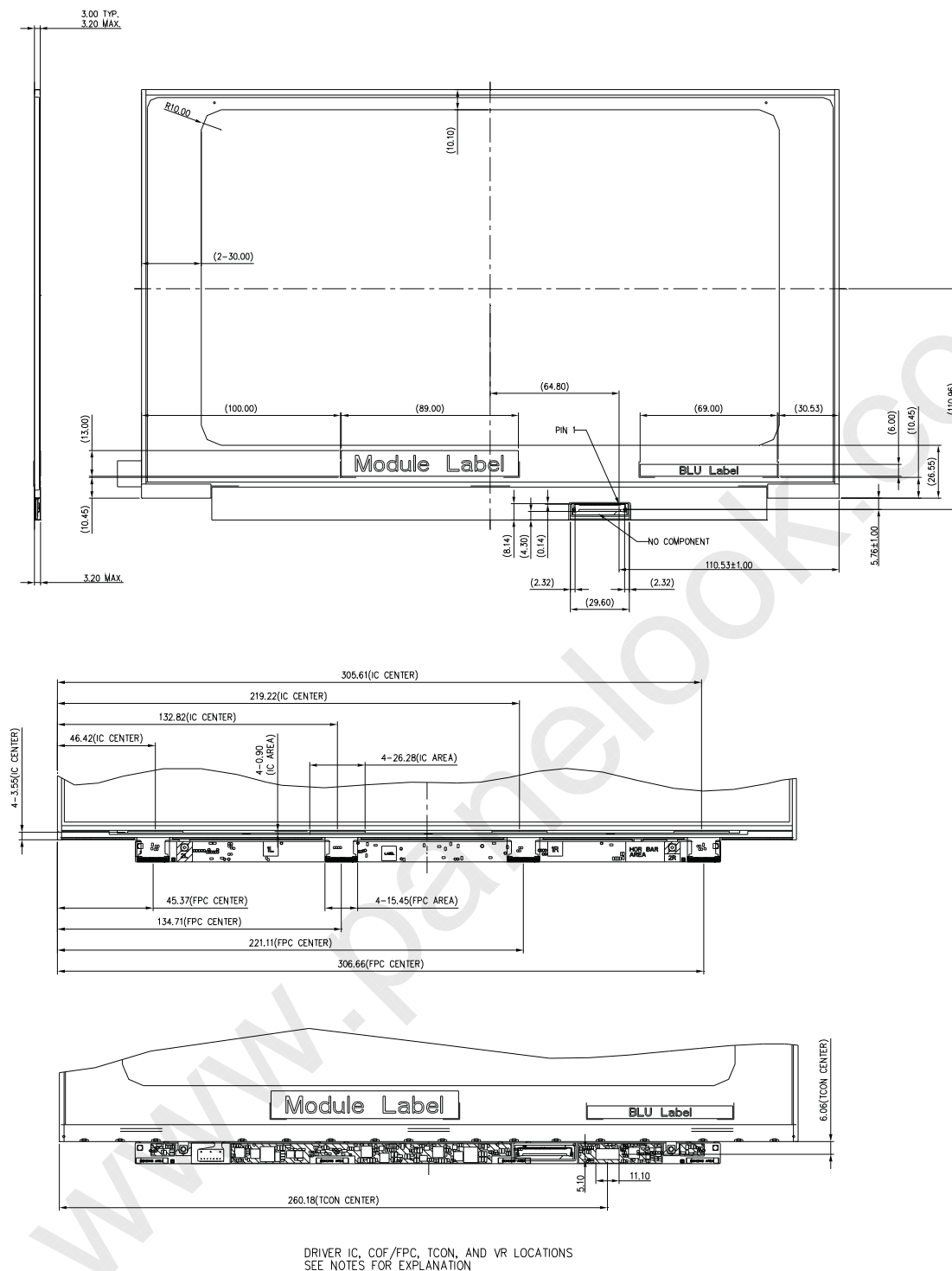
Appendix. OUTLINE DRAWING



NOTES:

1. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT, NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR FOREIGN OBJECTS OVER FPC/COF, T-CON AND VR LOCATIONS.
2. LVDS/EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
3. MODULE FLATNESS SPEC (0.5mm) MAX.
4. "()" MARKS THE REFERENCE DIMENSION.
5. LCD HIGHEST PORTION MUST BE TOP POLARIZER AND OTHER LCM MATERIALS MUST BE LOWER THAN TOP POLARIZER. THE SOP SHOULD REFER TO "DN0566762" IN INX.
6. MEASUREMENT OF THICKNESS MUST BE MEASURED BY CALIPER OR MICROMETER.

PRODUCT SPECIFICATION

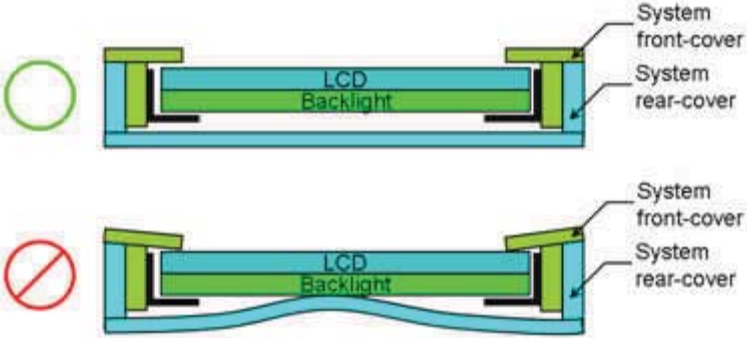
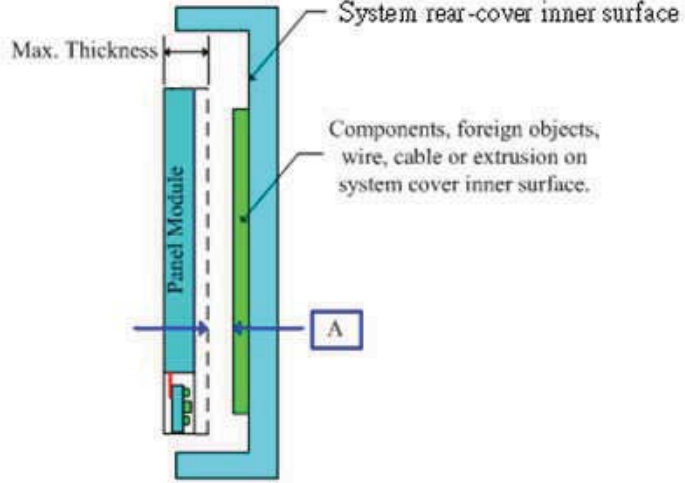


Note. Dimensions measuring instruments as below,

1. Length/ Width/Thickness : Caliper
2. Height : Height gauge
3. Flatness : Feeler gauge

PRODUCT SPECIFICATION

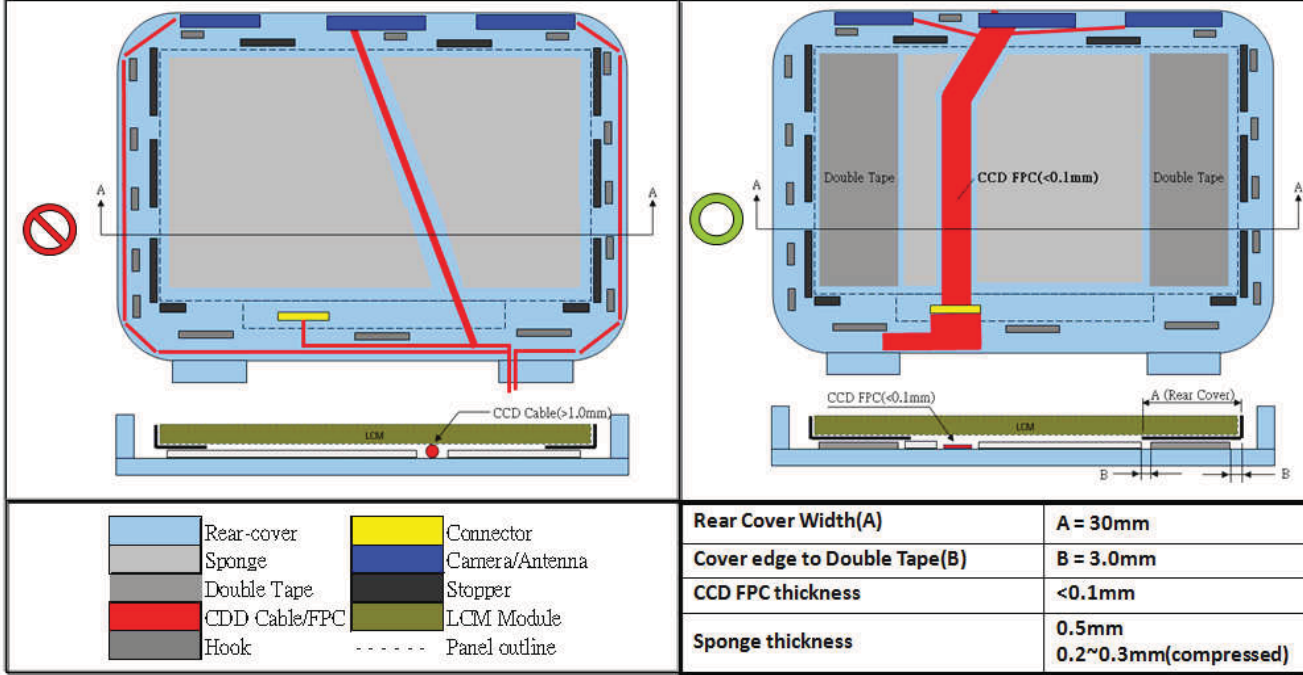
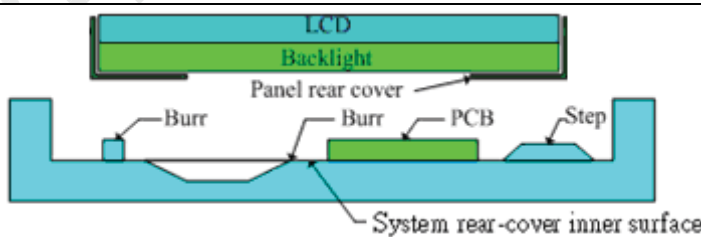
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	Permanent deformation of system cover after reliability test
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
1	Design gap A between panel & any components on system rear-cover
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Maximum flatness of panel and system rear-cover should be taken into account for gap design. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.

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2	Design gap C between system front-cover & panel surface.
	C:0.1mm MIN System front-cover LCD Backlight Panel rear-cover System rib higher than LCD module
Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.
3	Design gap D1 & D2 between system front-cover & PCB Assembly.
	D1:0.1mm MIN D2:2.0mm MIN System front-cover LCD Backlight PCB with components
Definition	Same as point 2 and 3, but focus on PCBA side.
4	Interference examination of antenna cable and WebCam wire
	Antenna WebCam WebCam Wire WebCam Wire BLU Label Module Label ok NG NG ok
Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may

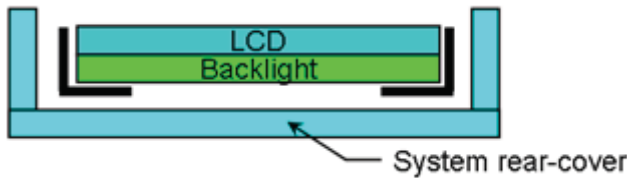
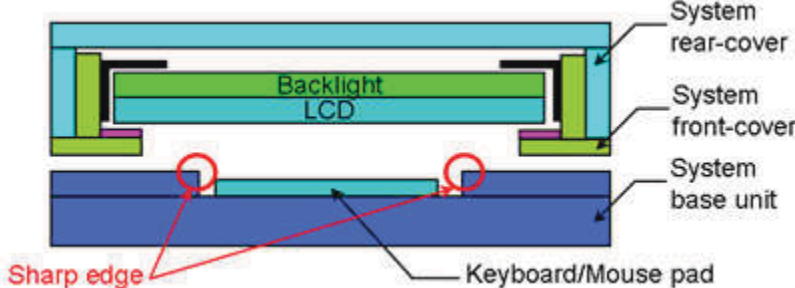
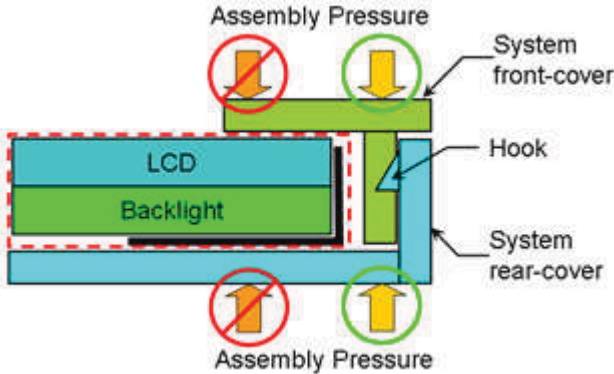
PRODUCT SPECIFICATION

	occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.																				
5	Interference examination of antenna cable and Web Cam wire - To prevent panel damage, we suggest using CCD FPC to replace CCD cable - Using double tape to fix LCM module for no bracket design.																				
	 <table border="1"> <tr> <td>Rear-cover</td><td>Connector</td></tr> <tr> <td>Sponge</td><td>Camera/Antenna</td></tr> <tr> <td>Double Tape</td><td>Stopper</td></tr> <tr> <td>CCD Cable/FPC</td><td>LCM Module</td></tr> <tr> <td>Hook</td><td>Panel outline</td></tr> </table> <table border="1"> <tr> <td>Rear Cover Width(A)</td><td>A = 30mm</td></tr> <tr> <td>Cover edge to Double Tape(B)</td><td>B = 3.0mm</td></tr> <tr> <td>CCD FPC thickness</td><td><0.1mm</td></tr> <tr> <td>Sponge thickness</td><td>0.5mm</td></tr> <tr> <td></td><td>0.2~0.3mm(compressed)</td></tr> </table>	Rear-cover	Connector	Sponge	Camera/Antenna	Double Tape	Stopper	CCD Cable/FPC	LCM Module	Hook	Panel outline	Rear Cover Width(A)	A = 30mm	Cover edge to Double Tape(B)	B = 3.0mm	CCD FPC thickness	<0.1mm	Sponge thickness	0.5mm		0.2~0.3mm(compressed)
Rear-cover	Connector																				
Sponge	Camera/Antenna																				
Double Tape	Stopper																				
CCD Cable/FPC	LCM Module																				
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Cover edge to Double Tape(B)	B = 3.0mm																				
CCD FPC thickness	<0.1mm																				
Sponge thickness	0.5mm																				
	0.2~0.3mm(compressed)																				
Definition	If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire.(Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC) Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.																				
6	System rear-cover inner surface examination																				
																					
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.																				

PRODUCT SPECIFICATION

7-1	Tape/sponge design on system inner surface
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.
7-2	Tape/sponge design on system inner surface
Definition	To prevent peeling the bezel tape in rework process. The length of double tape is $30 - (A+B)$, A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is $30-(2+2)=26\text{mm}$.

PRODUCT SPECIFICATION

8	Material used for system rear-cover
	 System rear-cover material: Al-Mg alloy System rear-cover thickness: 1.5mm MIN
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
9	System base unit design near keyboard and mouse pad
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
10	Assembly SOP examination for system front-cover with Hook design
	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.

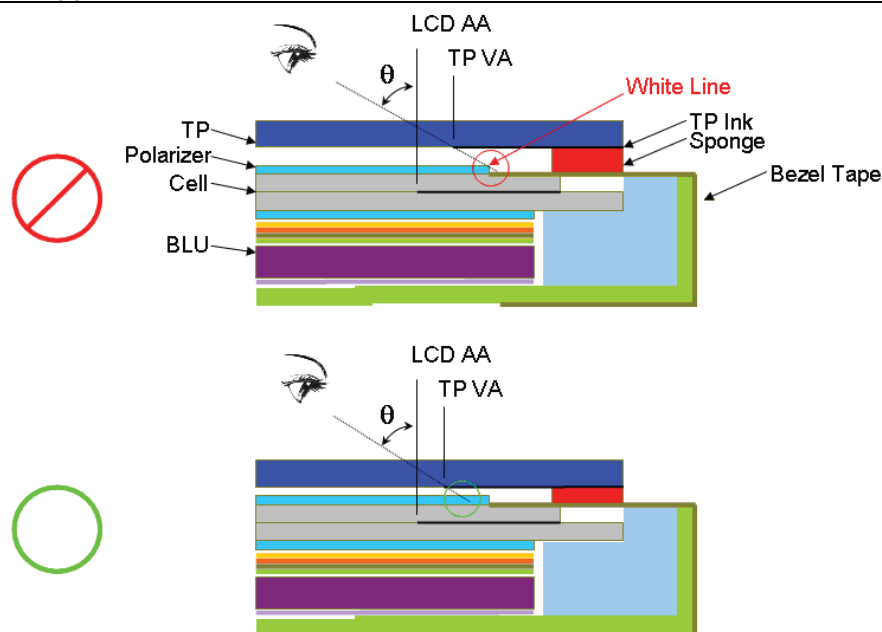
PRODUCT SPECIFICATION

11	Assembly SOP examination for system front-cover with Double tape design
Definition	To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do NOT put adhesive on CF pol.
12	System front-cover assembly reference with Double tape design
Definition	To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.
13	System front-cover opening area reference with TFT-LCD module
Definition	To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover edge more than 0.65mm.

PRODUCT SPECIFICATION

14

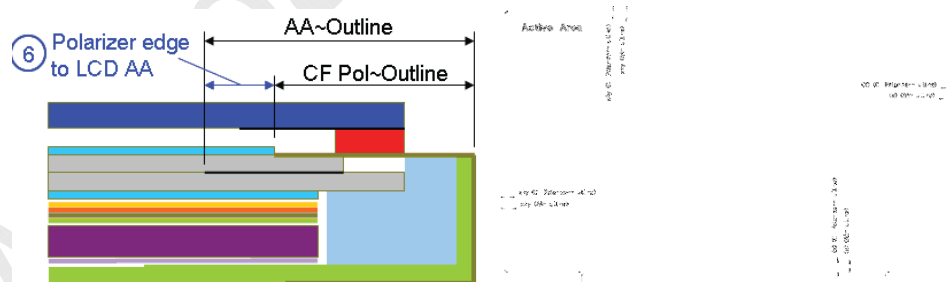
Touch Application : TP and LCD Module Combination for White Line Prevention



Parameter consideration for White Line Issue :

1	TP VA to LCD AA distance
2	TP Assembly tolerance
3	TP Ink Printing tolerance
4	Sponge thickness and tolerance
5	Inspection/Viewing Angle specification
6	Polarizer edge to LCD AA distance and tolerance

Polarizer edge to LCD AA distance can be derived by "AA~Outline" – "CF Pol~Outline" with respect to INX 2D Outline Drawing on each side.



Definition

For using in Touch Application: to prevent White Line appears between TP and LCD module combination, the maximum inspection angle location must not fall onto LCD polarizer edge, otherwise light line near edge of polarizer will be appear.

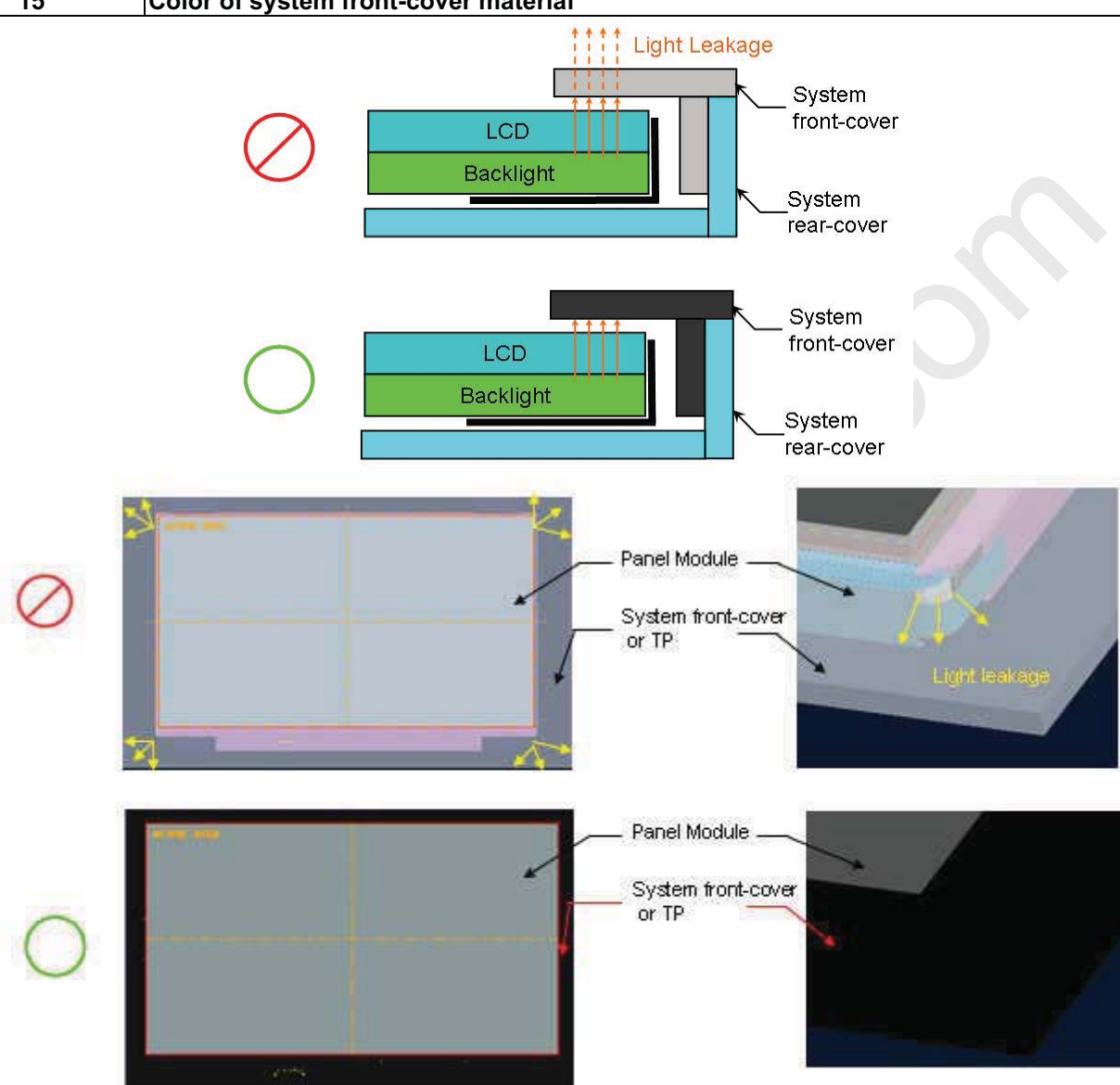
Parameters such as TP VA to LCD AA distance, TP assembly tolerance, TP Ink printing tolerance, Sponge thickness and tolerance, and Maximum Inspection/Viewing Angle, must be considered with respect to LCD module's Polarizer edge location and tolerance. This consideration must be taken at all four edges separately.

The goal is to find parameters combination that allow maximum inspection angle falls inside polarizer black margin area.

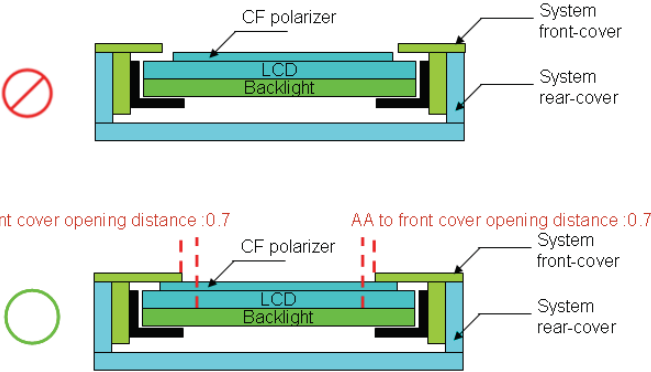
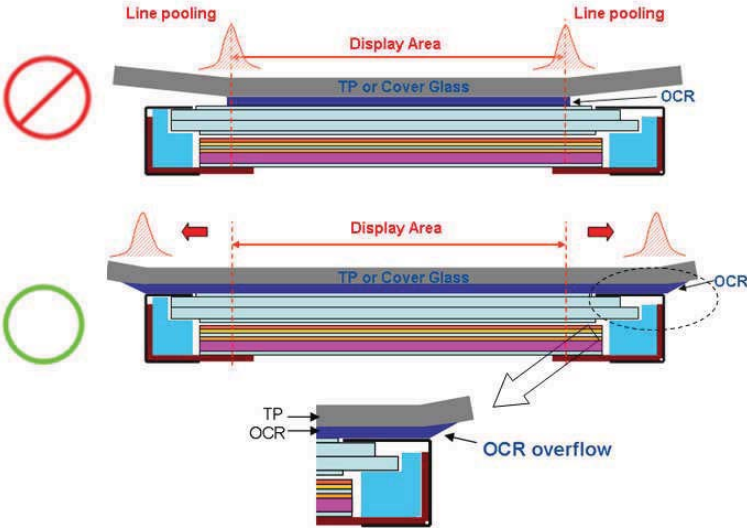
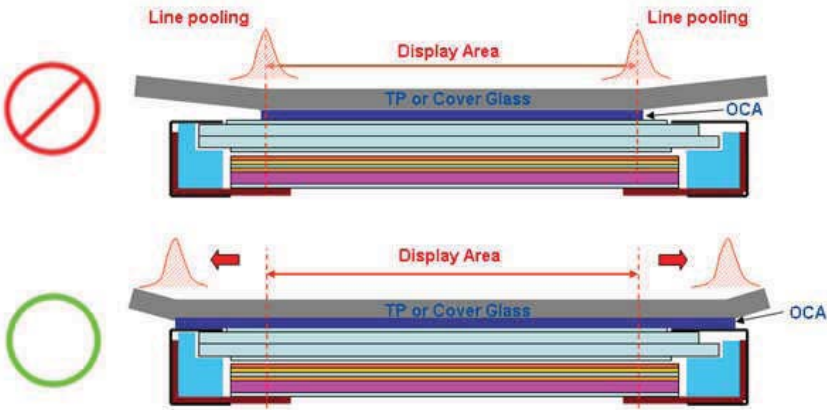
Note: Information for Polarizer edge location and its tolerance can be derived from INX 2D Outline Drawing ("AA ~Outline" - "CF Pol~Outline").

Note: Please feel free to contact INX FAE Engineer. By providing value of parameters above on each side, we can help to verify and pass the white line risk assessment for customer

PRODUCT SPECIFICATION

	reference.
15	Color of system front-cover material
 The diagrams illustrate the importance of using dark-colored material for the system front-cover to prevent light leakage. The top section shows a cross-section of the system with labels for 'LCD', 'Backlight', 'System front-cover', and 'System rear-cover'. It compares a light-colored front-cover (marked with a red 'X' for prohibition) which shows 'Light Leakage' (indicated by orange arrows), with a dark-colored front-cover (marked with a green circle for approval) which prevents leakage. The bottom section shows a top-down view of the 'Panel Module' and 'System front-cover or TP' (marked with a red 'X'), and a corresponding 3D cutaway view (marked with a green circle) showing 'Light leakage' (indicated by yellow arrows) from the light-colored front-cover, versus the dark-colored front-cover which prevents it.	
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

PRODUCT SPECIFICATION

16	AA to front cover opening distance
	
Definition	To prevent CF polarizer edge leakage .We suggest front cover opening no more than 0.7mm larger than active area on all 4 sides.
17	Use OCR Lamination
	
Definition	OCR glue as possible beyond module, in order to avoid Line Pooling
18	Use OCA Lamination
	
Definition	OCA glue as possible plastered throughout the module, in order to avoid Line Pooling.

PRODUCT SPECIFICATION

Appendix. LCD MODULE HANDLING MANUAL

Purpose	- This SOP is prepared to prevent panel dysfunction possibility through incorrect handling procedure. - This manual provides guide in unpacking and handling steps. - Any person which may contact / related with panel, should follow guide stated in this manual to prevent panel loss.
1.	Unpacking
  Open carton  Remove EPE Cushion   Open plastic bag  Cut Adhesive Tape  Remove EPE Cushion	
2.	Panel Lifting
 Remove PET Cover  Remove PE Foam  Handle with care (see next page)  Finger Slot Use slots at both sides for finger insertion. Handle panel upward with care.	

PRODUCT SPECIFICATION

3.

Do and Don't

Do :

- Handle with both hands.
- Handle panel at left and right edge.



Don't :

- Lifting with one hand.



- Handle at PCBA side.



Don't :

- Stack panels.



- Press panel.



Don't :

- Put foreign stuff onto panel



- Put foreign stuff under panel



PRODUCT SPECIFICATION

Don't :

- Paste any material unto white reflector sheet



Don't :

- Pull / Push white reflector sheet



Don't :

- Hold at panel corner.



Don't :

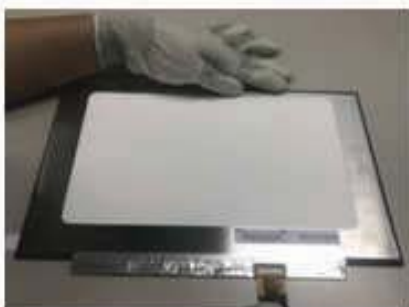
- Twist panel.



PRODUCT SPECIFICATION

Do :

- Hold panel at top edge while inserting connector.



Don't :

- Press white reflector sheet while inserting connector.



Do :

- Remove panel protector film starts from pull tape



Don't :

- Remove panel protector film From film another side.



PRODUCT SPECIFICATION

Don't :

- Touch or Press PCBA Area.

